SAUX

GEK-49283

OP-SV

GEK-49283

TermiNet*

LINE PRINTER
SERIAL CLOSED LOOP
BUFFERED AND UNBUFFERED
INTERFACE BOARD

SAUX

INSTRUCTION MANUAL

GENERAL ELECTRIC

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The information contained herein does not purport to cover all details or variations in equipment nor to provide for every possible contingency to be met in connection with installation, operation, or maintenance. Should further information be desired or should particular problems arise which are not covered sufficiently for the purchaser's purposes, the matter should be referred to General Electric Company, USA.

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SECTION 1

INTRODUCTION

GENERAL INFORMATION

This publication discusses the Serial Auxiliary (SAUX) circuit board. The SAUX can be installed in a TermiNet Line Printer to provide serial to parallel data conversion. When installed in a Line Printer, the SAUX is used in conjunction with either the Buffered or Unbuffered Parallel Interface circuit boards. The resulting combination forms either a Serial Buffered Closed Loop Interface, or a Serial Unbuffered Closed Loop Interface for the Line Printer. Communication between the SAUX and the data source is closed loop.

Both the Buffered (HINT) and Unbuffered (CINT) Interface circuit boards are discussed in publications GEK-35997 and GEK-49271. The use of a SAUX does not alter any basic information given in these publications, and that information will not be duplicated herein. When servicing a Line Printer with an SAUX/HINT or an SAUX/CINT interface, refer to the appropriate Interface board service manual and the appropriate Printer service manual.

DESCRIPTION OF BOARD

The Serial Auxiliary (SAUX) circuit board is designed to provide serial to parallel data conversion in a Buffered or Unbuffered Closed Loop Serial Interface configuration. The SAUX part number is 44C417545-G01. The SAUX contains circuitry which makes it signal level compatible with data systems employing EIA, TTL, or current loop data transfering techniques.

Data is received by the SAUX in bit serial character serial form from the data source. The speed of the data transfer is controlled by either a strap selectable internal baud rate clock, or an external clock signal from the data source. Parallel data is sent from the SAUX to the interface circuit board in bit parallel character serial form. Status signals from the parallel interface circuit board are received by the SAUX. These signals are modified and sent to the data source at the proper data level. Parity of the incoming data will be checked by the SAUX if a strapping option is exercised. Through the use of extensive strapping options, the SAUX/CINT and SAUX/HINT can be configured to allow the TermiNet Line Printer to function in many different hardware and software environments.

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SECTION 2

INSTALLATION

The SAUX circuit board is installed in the TermiNet Line Printer bustle slot labeled AUX. It engages the Printer Mother Board which interconnects it to the interface connector and to the parallel interface circuit board. The data source is connected by cable to the Line Printer interface connector. It is recommended that the interconnection cable be shielded, and that its length not exceed 50 feet (15.24 meters) for RS-232C and TTL interfaces.

SECTION 3

OPERATION

The basic operation of the Line Printer does not change when an SAUX board is used. The information provided in GEK-35997 and GEK-49271 still applies. Certain operation considerations apply when the SAUX is used in conjunction with the HINT and CINT interface boards. These considerations are discussed below.

SIGNAL LEVELS

The SAUX is designed to accept serial data transfer from a data source in several different ways.

1. In accordance with the EIA RS=232C Standard (excluding pin configuration)

2. TTL: Logic 0 = 0 to +0.4 volts
   Logic 1 = +2.4 volts to +5.5 volts
   Sink = 16 ma.
   Load = 400 na.

3. Current Loop: Current for both loops is supplied by the data source. The maximum loop voltage is +25 volts.
   Logic 0 = 0 to 5 ma.
   Logic 1 = 15 to 25 ma.

SECTION 4

PRINCIPLES OF OPERATION

The SAUX circuit board acts as a receiver for serial asynchronous data. It interconnects the normally parallel data TermiNet Line Printer with a data source configured to transmit serial data. Circuit design of the SAUX board is such that either the CINT or the HINT parallel Interface boards may be used in conjunction with it.

Input data is received serially and converted to parallel by a Serial to Parallel Converter. Parity of the input data is checked. The data baud rate clocking is derived by the SAUX board from the Printers 3.2 mHz oscillator signal. Provision is made to allow external clocking from data source as well. The SAUX board sends the converted parallel data to the parallel Interface board and generates the strobe signal which accompanies it.

Provisions are made on the various SAUX input line receivers and output line drivers, which connect to the data source, to make them level compatible with EIA RS-232C, TTL and Current Loop signals. These lines communicate Printer status, data source control information, and recieved data.

Extensive strapping options available on the SAUX board allow the Line Printer to be compatible with many different data source configurations. They also allow variations in the data handling with Interface boards.

CIRCUIT OPERATION

The detailed circuit analysis of the SAUX board is given in the paragraphs below. The discussion is based upon the block diagram shown in Figure 4-1.

RATE MULTIPLIER

The Rate Multiplier derives the internal baud rate clocking signals from the 3.2 mHz oscillator signal sent to it from the Printer LOG board. The circuit takes the basic 3.2 mHz input signal and through its various counting stages derives the following clock rates: 9600, 4800,. 2400, 1200, 600, 300, 220, and 150. These various clock rate signals are applied to the Clock Gate through a strap field as the signal Receive Rate Clock (RRC).

Applied to the Rate Multiplier is the signal $\overline{\text{BAUD CK ENABLE}}$ generated by the Baud Clock Enable circuit. This signal will disable the generation of RRC whenever it is taken to a logic 0.

EXTERNAL CLOCK RECEIVER

The External Clock Receiver receives a clock signal from the data source if one is sent. The circuit is designed to accept TTL or EIA signals. The input signal is conditioned, if required, to a level acceptable to the SAUX board. The conditioned signal is gated and sent to the Clock Gate. Whenever an external clock is desired the internal clock must be disabled through a strap option in the Rate Multiplier circuit.

Strapping options in the Clock Receiver, can be adjusted for the particular type of clock input supplied and for the logic level used to trigger the Clock Gate.

CLOCK GATE

The Clock Gate is designed to receive clocking signals from the Rate Multiplier or the External Clock Receiver. From these signals, it generates the BAUD CLOCK signal.

The clocking signals are synchronized with the 3.2 mHz LOG board oscillator signal. This is done to eliminate any delay which may have been introduced by the Rate Multiplier during its derivation process. Or, in the case of the external clock, this action synchronizes the clock signal with the remaining Printer circuit timing. The generated BAUD CLOCK signal is sent to various SAUX board circuits to provide their timing. It is sent to the S/P Converter to determine the speed at which data is passed to the SAUX board from the data source.

DATA RECEIVER

Serial data is applied to the SAUX board from the data source through the Data Receiver circuit. Serial data may be supplied at either TTL, EIA or Current Loop levels. The applied serial data is level conditioned, gated, and sent to the S/P Converter as Internal Received Data (IRD). Its compliment, $\overline{\text{IRD}}$, is also generated to be used by the parity checking circuits.

IRD is clocked into the S/P Converter from the Data Receiver by the BAUD CLOCK signal. The actual data sampling occurs during the middle of each IRD data bit.

PRIMING GENERATOR

The Priming Generator receives two clearing signals from the data source. These signals are only generated when an EIA RS232C type of data source is being employed. These signals, when active, will prevent the Printer from accepting data from the data source and will force the SAUX into a cleared state.

The signal INTERFACE ENABLE 1 or INTERFACE ENABLE 2 is applied as a negative signal pulse when active. The signal is level conditioned and gated to enable the output signal PRIME. The PRIME signal is sent to a CINT Interface to clear its circuits. PRIME has no effect on the HINT board. The PRIME signal is also sent to the Clear Generator where it is gated to generate the CLEAR signal.

When the INTERFACE ENABLE 1 signal is not active, the Priming Generator generates the Ready To Printer (RTP) signal. The RTP signal causes the Printer READY light to turn on when an HINT Interface is being used.

HALF BIT SUPPRESSOR

The Half Bit Suppressor circuit is designed to prohibit the SAUX Board from responding to noise pulses less than one half bit wide on the data line. The circuit monitors the Internal Received Data Signal (IRD) and the BAUD CLOCK signal.

The Suppressor monitors the first half of each IRD character start bit. If the IRD signal is a character start bit, it will stay in a steady logic state until the BAUD CLOCK signal is applied one half bit time later. In this case, the Half Bit Suppressor takes no action. The circuit will be reinitialized by the Series/Parallel Clear (S/P Clear) signal when the complete present received character has passed through the SAUX circuit.

The applied IRD signal could be a short noise pulse whose logic state does not remain steady until the BAUD CLOCK signal is applied one half bit time later. In this case, the Suppressor will generate a SUPPRESS signal. The SUPPRESS signal is applied to the Clear Generator where it is gated to generate the CLEAR signal. Since the CLEAR signal inhibits the Baud Clock Enable circuit, the BAUD CLOCK will not be generated and the noise pulse will not be accepted as data.

CLEAR GENERATOR

The Clear Generator is a gating circuit which generates a CLEAR Signal. The CLEAR signal, when generated, will prevent the SAUX board from accepting data. It does this by inhibiting the Baud Rate Enable Circuit which, in turn, inhibits the generation of the BAUD CLOCK Signal by the Rate Multiplier.

CLEAR is generated when any of the following signals are applied to the circuit input: SUPPRESS from the Half Bit Suppressor, PRIME from the Priming Generator, STOP DELAYED from the Series/Parallel Converter, or LV from the Printer LOG Board.

SERIAL TO PARALLEL CONVERTER

The S/P Converter is a shift register which receives a serial data character bit by bit, shifts the bits through its stages, and presents the character bits in parallel on its output lines. The shifting is clocked by the BAUD CLOCK signal pulses from the Clock Gate circuit.

At Printer power up time, the S/P Converter is cleared and initialized. The initialization results in a tag bit resting in the first stage of the shift register of the S/P Converter. The start bit of the received character is presented to the S/P Converter input from the Received Data Interface on the Internal Receive Data (IRD) line. At BAUD CLOCK pulse time it is shifted into the first shift register. The tag bit resting there is shifted to the next register. At each BAUD CLOCK pulse time, an additional bit of the received character is clocked into the S/P Converter.

When the tag bit is shifted into the tenth shift register, the S/P Converter generates the PARITY signal. This signal is sent to the Parity Enable circuit to enable it. This action causes the Data Buffer to be enabled by the Parity Enable circuit. The tag bit, start bit and eight data bits now reside in the S/P Converter registers. As soon as the Data Buffer is enabled, the eight data bits are sent in parallel to it from the S/P Converter over data lines DB1-DB8.

When the stop bit is clocked into the S/P Converter, the tag bit is shifted into the eleventh shift register. This action causes the signals STOP and STOP DELAYED to be generated. The STOP signal is sent to

Parity Enable circuit to clear the circuit. At the same time, the STOP DELAYED, signal is sent to the Clear Generator circuit to cause it to generate and send CLEAR to the Baud Clock Enable circuit. The Baud Clock Enable circuit then generates and sends the S/P CLEAR signal to the S/P Converter. The signal clears and reinitialized the Converter's shift registers. The S/P Converter is now ready to accept the next received data character.

PARITY ENABLE

The Parity Enable circuit is responsible for generating signals which enable the Data Buffer and the Parity Out Gate.

When bit 10 of the received character is clocked into the S/P Converter, it generates PARITY and sends it to the Parity Enable circuit. The PARITY signal, when received, causes the Parity Enable circuit to generate the signals Internal Clock (I Clock) and ENABLE. I CLOCK is sent to the Data Buffer where it enables the Buffer to accept the eight data bits from the S/P Converter. The ENABLE signal is sent to the Parity Out Gate where it enables the Gate and allows parity status to be sent to the data source.

When the 11th bit of the received character is clocked into the S/P converter, the converter generates the STOP signal. The STOP signal is sent to the Parity Enable circuit. When received, STOP causes the circuit to turn off the generated I Clock and ENABLE signals. The Parity Out Gate is disabled by the turning off of the ENABLE signal.

PARITY CLEAR CIRCUIT

The Parity Clear Circuit is responsible for clearing the Parity Generator after the parity status has been sent to the data source through the Parity Out Gate. The Parity Clear signal monitors the ENABLE signal from the Parity Enable circuit and gates it with the BAUD CK ENABLE signal from the Baud Clock Enable circuit.

When the Parity Enable circuit receives STOP from the S/P Converter, it turns off the ENABLE signal to the Parity Clear circuit. A short time later the BAUD CK ENABLE signal is applied by the Baud Clock Enable circuit. At this time, the PARITY CLEAR signal is generated and sent to the Parity Generator.

The sequence of action is such that the Parity Out Gate is disabled before the Parity Generator is Cleared.

PARITY GENERATOR

The Parity Generator generates a PARITY STATUS signal for each received character. The Parity Generator is configured such that whenever a 1 bit is applied on the IRD input, the circuit output signal changes states when the data is sampled. Depending upon the placement of certain strapping options a logic 1 or a logic 0 parity status (for even or odd parity) signal is sent to the Parity Out Gate.

After the Parity Enable circuit is cleared by the S/P Converter, the Parity Clear circuit combines the ENABLE and BAUD CK ENABLE signals to produce the PARITY CLEAR signal. The PARITY CLEAR signal is sent to the Parity Generator to clear it. The Parity Generator is cleared at the same time the S/P Converter is reinitialized. The result of this action is to allow the Parity status to remain stable until after the Parity Out Gate and the baud rate clock has been disabled.

Allowing the parity status to become stable before the Gate is enabled, and holding it stable until after the gate is disabled, insures the PARITY ERROR signal will be a clean switch free of any logic racing effect.

The Parity Generator is time by the BAUD CLOCK generated by the Clock Gate circuit.

PARITY OUT GATE

The Parity Out Gate allows a parity status signal to be transmitted to the data source from the Parity Generator. The status is conveyed by the PARITY ERROR status line.

The Parity Out Gate is enabled by the Parity Enable circuit through its generated ENABLE signal. Once enabled, the PARITY STATUS signal from the Parity Generator is gated to the data source over the PARITY ERROR status line. The line is taken positive to indicate a parity error, or held at 0 to indicate good parity. A strapping option in the Gate circuit
determines the timing relationship of the parity status signal.

The Parity Out Gate generates a Parity Error Detected (PED) signal when a parity error is determined. PED is sent to the Data Buffer to force a Delete character on its output data lines. PED is also sent to the Data Strobe circuit where it can be strapped to inhibit the generation of a data strobe signal.

BAUD CLOCK ENABLE

The Baud Clock Enable circuit provides a logic signal which enables the baud rate clock. It also provides a signal to clear the S/P Converter at the proper time. The circuit is clocked by the start bit of the Internal Received Data (IRD) signal.

The IRD start bit causes the $\overline{\text{BAUD CK ENABLE}}$ to switch to a logic 1 level. The $\overline{\text{BAUD CK ENABLE}}$ signal is sent to the Rate Multiplier circuit to allow the baud rate clock to be generated. The signal remains at the level until the IRD stop bit is clocked into the S/P Converter.

When the IRD stop bit is clocked into the S/P Converter, the converter generates the signal STOP DELAYED and send it to the Baud Clock Enable circuit. The Baud Clock Enable circuit changes its $\overline{\text{BAUD CK ENABLE}}$ signal to a logic 0. This action resets and inhibits the Rate Multiplier from generating the baud rate clock signal. The Baud Clock Enable circuit at this time also generates S/P CLEAR. The S/P CLEAR signal is sent to the S/P Converter to clear its registers.

The above action also happens if the Clear Generator generates the CLEAR signal and sends it to the Baud Clock Enable circuit. By doing this, extraneous noise pulses on the data line are not responded to by the SAUX circuit board. The CLEAR signal is also sent when the data source has commanded the SAUX board to not accept received data, or during a Printer low voltage condition.

DATA BUFFER

The Data Buffer is composed of an eight bit latch. It is designed to buffer one data character.

When the signal Internal Clock (I CLOCK) is generated and sent from the Parity Enable circuit, the Buffer is enabled. Once enabled, the Buffer accepts a parallel data character from the S/P Converter. It does this by receiving individual bits of the data character in parallel form on data lines $\overline{\text{DB1}}$ through $\overline{\text{DB8}}$.

The buffered data character is transmitted from the Data Buffer to the Interface board over output data lines D1-D8. This action occurs when a data strobe signal is generated and sent to the Interface board by the Data Strobe circuit. Once a character is strobed to the Interface from the Data Buffer, another character can be written over the present buffered character information.

A provision is made to allow a parity error to force a Delete character into the Data Buffer. The Parity Error Detected (PED) signal is supplied by the Parity Out Gate for this purpose. This action allows the Printer with a CINT interface board to print a diamond when a parity error is detected. The Printer must be so configured and certain strapping options must be selected on the SAUX board.

DATA STROBE

The Data Strobe circuit is responsible for generating the strobe signal. The strobe signal is required for data to be accepted by the HINT or CINT Interface board.

The Data Strobe circuit generates STROBE (STB) in response to a strap selectable input. Depending upon the strap placement, either Internal Clock (I CLOCK) from the Parity Enable circuit or STOP DELAYED from the S/P Converter causes STB to be generated.

The $\overline{\text{BUSY}}$ signal, applied to the Strobe circuit by the Busy Generator as a logic 1, enables the generation of the STB signal. Conversely, a $\overline{\text{BUSY}}$ = 0 will disable the generation of STB while a Printer BUSY status exists. One more character may be accepted from the data source after Busy comes true. It will be stored in the Data Buffer. The STB associated with this character will be enabled and held until the BUSY signal goes away. At this time, it will be generated.

The Parity Error Detected (PED) signal from the Parity Out Gate may optionally be strapped to inhibit STB if a received character has a parity error. If strapped otherwise, and STB will be generated even though the character has a parity error. By allowing STB to be generated when a parity error exists, a Delete character which is forced into the Data Buffer can be strobed to the Interface Board. Because of this, a Printer with a CINT Interface can print a diamond when a parity error is detected. The Printer must be so configured and certain strapping options must be in place on the SAUX Board.

DELETE DETECTOR

The Delete Detector circuit is designed to disallow a received Delete character from being sent to the

Interface board from the SAUX board. It will, however, allow an internally generated Delete character to be sent. The Delete Detector action is dependent upon certain strapping options.

The Delete Detector monitors the output data lines D1-D7 from the Data Buffer. It also monitors the Parity Error Detected (PED) signal from the Parity Out Gate. A Delete character is applied to the Detector circuit every time one is placed in the Data Buffer. If the Delete character was received from On Line in correct parity, the PED signal will allow the Detector to generate Delete Decoded ($\overline{DEL}$). The $\overline{DEL}$ signal is sent to the Data Strobe circuit where it inhibits the generation of the STROBE (STB) signal. Therefore, a correctly received Delete character will not get strobed to the Parallel Interface board. This allows the Parallel Interface to distinguish between a received $\overline{DEL}$ and one generated because of a parity error.

A Delete code may be resident in the Data Buffer because it was forced there when any character was received with a parity error. In this case, the PED signal inhibits the Delete Detector, DEL is not generated, and STB is generated. This forced Delete character does get strobed to the Parallel Interface board. It may cause a Printer with a CINT Interface to print a diamond if it is configured to do so, and if certain strapping options are in place on the SAUX board.

ETB DETECTOR

The ETB Detector allows the Printer to empty the First In First Out (FIFO) buffer on the HINT Interface board through the use of a control code. This action is enabled by the installation of a strapping option.

The ETB Detector is configured such that a received ASCII ETB code is decoded when the Detector circuit is enabled by the Strobe (STB) signal. The decoded signal triggers a timer and casuses ETB Detected (ETB D) to be generated. The ETB D signal is sent to the Busy Generator circuit to cause BUSY to be generated and sent to the Data Source. When the timer times out, the BUSY signal to the data source is removed. The time out period of approximately 47 msec. allows the HINT FIFO to empty while BUSY to the data source is true.

If data is being transfered from the FIFO to the Printer LOG board when an ETB code is detected, the signals Transfer ($\overline{XFR}$) and Data Strobe (DSTB) from the Parallel Interface will not allow the timer to time out. If the Printer is printing or the Parallel Interface is busy, the signal Interface Busy (I BUSY) will prohibit the timer from timing out. In each of the above cases the BUSY signal is sent to the data source until the action is complete.

BUSY GENERATOR

The Busy Generator is a gating arrangement which receives the BUSY signal from the Interface board. A strapping option allows either an HINT or a CINT board BUSY input. Also applied, is the ETB Detected (ETB D) signal from the ETB Detector circuit, and the Low Paper (LOPX) signal from the Status Receiver circuit. Any of these inputs causes an output BUSY signal to be generated and sent to the data source.

The output BUSY signal from the Busy Generator is strap selectable as to its logic state. The output BUSY signal is available at EIA and TTL voltage levels and Current Loop current levels. In addition to the BUSY signal sent to the data source, teh Interface Busy (I BUSY) and $\overline{BUSY}$ signals are generated for use on the SAUX Board. I BUSY is sent to the ETB Detector to disable it, and $\overline{BUSY}$ is sent to the Strobe Generator to inhibit data strobe generation.

The Busy Generator drives a board mounted Light Emitting Diode (LED). The LED is turned on whenever BUSY is generated.

STATUS RECEIVER

The Status Receiver circuit receives certain Printer status information conditions it, and communicates it to the data source. Applied to the Status Receiver is the FAULT signal from either the HINT or CINT Interface boards. A strapping option allows either input. The output of the Status Receiver is the $\overline{FAULT}$ signal. The $\overline{FAULT}$ signal is gated and conditioned to the proper level. It is sent to the data source through an enabling strap option.

The Low Paper ($\overline{LOPX}$) signal from the Printer Low Paper Sensor is applied to the Status Receiver. It is gated, level conditioned, and sent to the data source through an enabling strap option as $\overline{LOW\ PAPER}$. The $\overline{LOPX}$ signal is also buffered by the circuit and sent to the Busy Generator to cause BUSY to be generated. The FAULT and $\overline{LOPX}$ signals are gated together to produce a FAULT·LOPX signal. This signal is sent to the Status Line Driver circuit to inhibit the PRINTER READY signal.

STATUS LINE DRIVER

The Status Line Driver circuit provides a Printer status signal to the data source. This signal indicates the Printers ability to accept data.

Depending upon which Interface board is being used (HINT or CINT), either an ON LINE or a SELECT status signal is applied to the Status Line Driver. Either input is strap selected. When the Driver circuit receives a Printer status signal, it generates a level conditioned PRINTER READY signal. The PRINTER READY signal is sent to the data source.

Also applied to the Status Line Driver circuit is the FAULT·LOPX signal from the Status Receiver circuit. If a Printer fault or low paper condition exists, FAULT·LOPX will inhibit the generation of PRINTER READY.

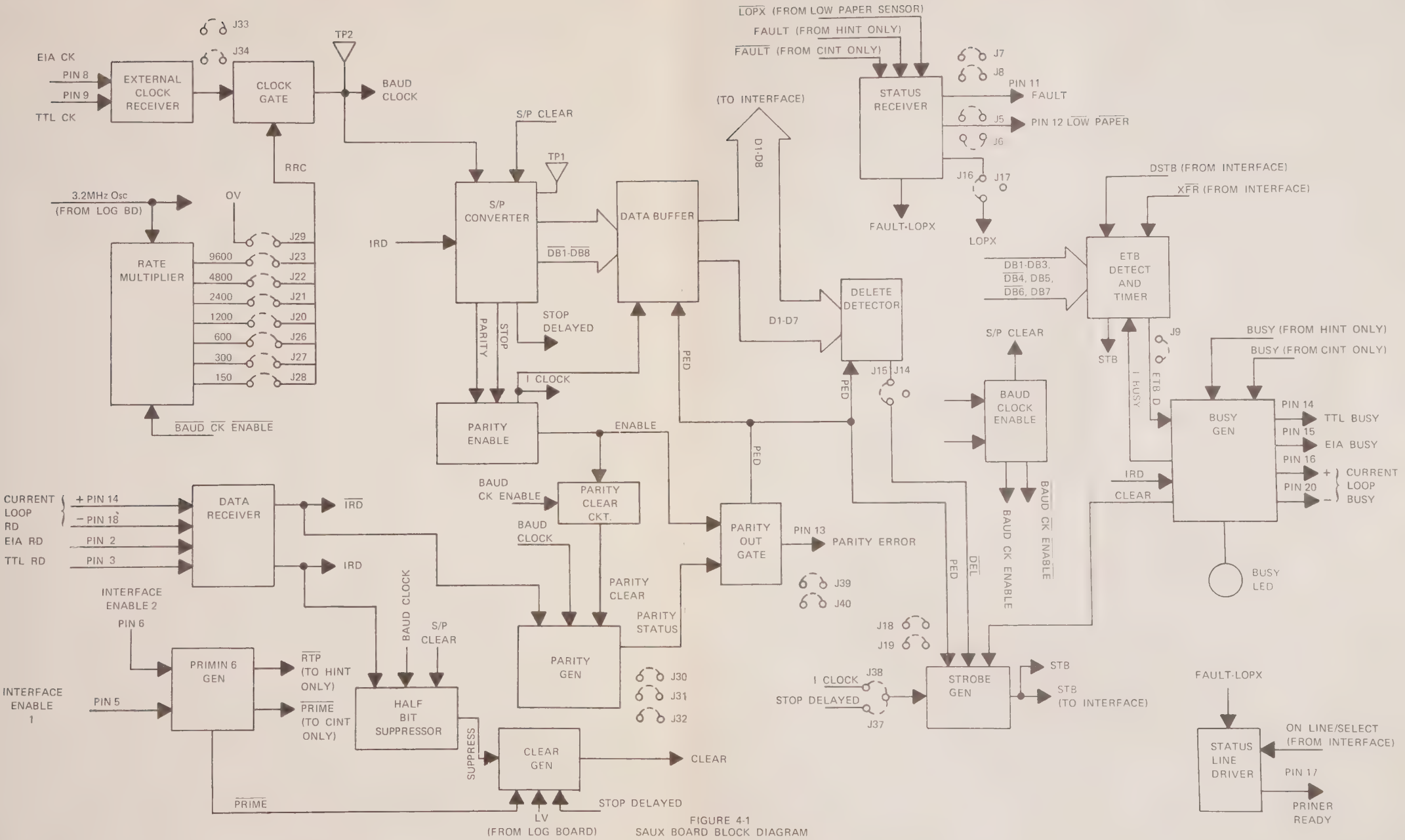

FIGURE 4-1
SAUX BOARD BLOCK DIAGRAM

SECTION 5

MAINTENANCE

PREVENTIVE

There are no preventive maintenance precautions which concern the SAUX circuit board in particular. Any and all information provided in Section 5 of GEK-35997 and GEK-49271 and Chapter 5 of the appropriate Printer service manual does apply.

TROUBLESHOOTING

STATUS INDICATOR

The SAUX contains one LED status indicator. This board mounted LED is a BUSY indicator. When the Printer is able to accept data from the data source, this LED will be off. When the Printer cannot accept data from the data source, the BUSY LED will be lit.

INTERFACE SIGNALS

The tables below (Table 5-1, 5-2, and 5-3) illustrate the pin assignments of the interface connector between the data source and the SAUX board.

TABLE 5-1

EIA INTERFACE CONNECTOR PIN ASSIGNMENT

SIGNAL ROUTING	PIN NO.	SIGNAL NAME	LOGIC STATE WHEN ACTIVE
SIGNALS TO PRINTER	2	Received Data	RS-232C Standard Serial by bit. Serial by character.
	5	Interface Enable 1	Negative voltage. Will prevent SAUX from accepting data. Will be positive if unterminated by data source. Positive voltage causes READY light to be lit on control panel when HINT Interface board is used.
	6	Interface Enable 2	Same as above but does not affect control panel light.
	7	Logic 0	RS-232C Standard.
	8	Baud Rate Clock	RS-232C Standard. 110 - 9600 baud.
	1	Frame Ground	Cable Shield.
	7	Logic 0	RS-232C Standard.
	11	Fault	Negative voltage. Indicates that a Printer alarm condition exists. Strap option allows low paper condition to generate FAULT, as well.

SIGNAL ROUTING	PIN NO.	SIGNAL NAME	LOGIC STATE WHEN ACTIVE
SIGNALS FROM PRINTER	12	Low Paper	Negative voltage. Indicates that a Printer low paper condition exists. Strap option allows alarm condition to generate LOW PAPER, as well.
	13	Parity Error	Positive voltage for one bit time when parity error is detected. Parity dectc-tion strap enabled. Signal active timing strap selected.
	15	BUSY	Active logic level strap selected to a positive or negative RS-232C level. Indicates when Printer can receive data.
SIGNALS FROM PRINTER	17	Printer Ready	Positive voltage. Indicates when Printer is On Line (Selected). Also indicates alarm and low paper con-ditions do not exist.
NOTE: A simple EIA Interface can be configured using only pins 1, 2, 7, and 15.			

TABLE 5-2

TTL INTERFACE CONNECTOR PIN ASSIGNMENT

SIGNAL ROUTING	PIN NO.	SIGNAL NAME	LOGIC STATE WHEN ACTIVE
SIGNALS TO PRINTER	3	Received Data	Logic 1 = 2.4V to 5.5V. Logic 0 = 0 to 0.4V. Serial by bit. Serial by character.
	7	Logic 0	0 to 0.4 volts.
	9	Baud Rate Clock	Square wave 50% duty cycle TTL level signal.
SIGNALS FROM PRINTER	1	Frame Ground	Cable Shield.
	7	Logic 0	0 to 0.4 volts.
	14	BUSY	Active logic level strap selectable to positive or negative TTL level indi-cates when printer can receive data.

TABLE 5-3

CURRENT LOOP INTERFACE CONNECTOR PIN ASSIGNMENT

SIGNAL ROUTING	PIN NO.	SIGNAL NAME	LOGIC STATE WHEN ACTIVE
SIGNALS TO PRINTER	4	+ Received Data	Current Loop Logic 1 = 15 to 25 ma. Logic 0 = 0 to 5 ma. Serial by bit. Serial by character.
	18	- Received Data	
	1	Frame Ground	Cable Shield.
	16	+ Busy	Current Loop. Active logic level strap selectable to logic 1 or logic 0 current level. Indicates when Printer can receive data.
	20	- Busy	
NOTE: Current povided by data source.			

STRAPPING OPTIONS

Certain strapping options are available on the SAUX which will allow the Printer to interface into different hardware and software requirements. SAUX strap arrangement differs depending upon which Interface board is used. Strapping arrangements on the CINT and HINT must be in a certain configuration when the SAUX is used.

The following tables (Table 5-4 and 5-5) detail the SAUX strapping arrangement when an HINT or a CINT board is used. HINT and CINT strapping requirements are detailed as well. Standard strapping as shipped from the factory are marked with an asterick.

TABLE 5-4

SAUX STRAPPING OPTIONS WHEN USED WITH THE HINT INTERFACE BOARD

DESCRIPTION OF STRAPPING OPTION		STRAP REQUIRED	STRAP POSITION
Allows Buffered Closed Loop Serial Operation		*J1, J3, J11 J12, & J15	IN
		J2, J4, J10, J13, J14	OUT
LOW PAPER Signal reflects:	Low paper condition only.	*J5	IN
		*J6	OUT
	Low paper and fault condition.	J5	OUT
		J6	IN
	Low paper and fault condition.	J7	IN
		*J8	OUT

(TABLE 5-4 CONTINUED)

DESCRIPTION OF STRAPPING OPTION		STRAP REQUIRED	STRAP POSITION
	Fault condition only.	*J7	OUT
		*J8	IN
ETB code	Causes a BUSY to be generated until the HINT buffer is empty. Is ignored.	J9	IN
		*J9	OUT
LOW PAPER SENSOR activation:	Causes Busy to inhibit data flow from data source.	J16	OUT
		J17	IN
	Does not affect data flow.	*J16	IN
		*J17	OUT
Character printed when received with Parity Error.	Character printed as received	J18	IN
		J19	OUT
	Nothing printed - not even a space.	*J18	OUT
		*J19	IN
Baud Rate Clock selection.	External Clock	J29	IN
		J20, J21, J22, J23, J26, J27, & J28	OUT
	150 Baud	J28	IN
		J20, J21, J22, J23, J26, J27, & J29	OUT
	300 Baud	J27	IN
		J20, J21, J22, J23, J26, J28, & J29	OUT
	600 Baud	J26	IN
		J20, J21, J22, J23, J27, J28, & J29	OUT
	1200 Baud	J20	IN
		J21, J22, J23, J26, J27, J28, & J29	OUT
	2400 Baud	J21	IN
		J20, J22, J23, J26, J27, J28, & J29	OUT

*Standard Strapping configuration as shipped from the factory.

(TABLE 5-4 CONTINUED)

DESCRIPTION OF STRAPPING OPTION		STRAP REQUIRED	STRAP POSITION
	4800 Baud	J22	IN
		J20, J21, J23, J26, J27, J28, & J29	OUT
	9600 Baud	*J23	IN
		J20, J21, J22, J26, J27, J28, & J29	OUT
Parity Detection	Even	J30	IN
		J31, J32	OUT
	Odd	J31	IN
		J30, J32	OUT
	Disabled	*J32	IN
		*J30, J31	OUT
BUSY signal status when Printer cannot accept data	EIA negative. TTL Low. No Current in Loop.	J24	OUT
		J25	IN
	EIA Positive. TTL High. Current in Loop.	*J24	IN
		*J25	OUT
Allows EIA or Current Loop configuration with TTL level external baud rate clock, and with data sampling at high to low transition.		*J33	IN
		*J34	OUT
Same as above, except data sampling is at low to high transition.		J33	OUT
		J34	IN
Allows EIA or Current Loop configuration with TTL received data signal at low level for binary 1 (start bit high)		*J35	OUT
		*J36	IN
Same as above except TTL received data signal is at high level for binary 1 (start bit low)		J35	IN
		J36	OUT
BUSY signal transition	Middle of stop bit	J37	IN
		J38	OUT
	Middle of parity bit	*J37	OUT
		*J38	IN

*Standard Strapping configuration as shipped from the factory.

(TABLE 5-4 CONTINUED)

DESCRIPTION OF STRAPPING OPTION		STRAP REQUIRED	STRAP POSITION
Parity Error signal duration	Middle of stop bit of erroneous character to middle of start bit of next character.	*J39	IN
		*J40	OUT
	Middle of parity bit to middle of stop bit of erroneous character.	J39	OUT
		J40	IN

HINT STRAPPING

The strapping of the Buffered Parallel Interface (HINT) circuit board is described in GEK-35997. When the HINT is used in conjunction with the SAUX, its strapping is arranged as explained below.

To allow Buffered Closed Loop Serial Operation:
Strap J2, J3, & J19 must be IN
Strap 1 & 20 must be OUT

In addition to the above requirements, normal strapping (as shipped from the factory) of the remaining straps are:
J13, J21, J23, J26, J29, J31, & J33 IN*
J11, J12, J22, J24, J27, J30, J32, & J34 OUT*

*Standard strapping configuration as shipped from the factory.

TABLE 5-5

SAUX STRAPPING OPTIONS WHEN USED WITH THE CINT INTERFACE BOARD

DESCRIPTION OF STRAPPING OPTION		STRAP REQUIRED	STRAP POSITION
Allows Unbuffered Closed Loop Serial Operation		*J2, J4, J13, J17,	IN
		J1, J3, J12, J9, & J16	OUT
LOW PAPER signal reflects:	Low paper condition only.	*J5	IN
		*J6	OUT
	Low paper and fault conditions.	J5	OUT
		J6	IN
FAULT signal reflects:	Low paper and fault condition.	J7	IN
		J8	OUT
	Only fault condition.	*J7	OUT

*Standard strapping configuration shipped from the factory.

(TABLE 5-5 CONTINUED)

DESCRIPTION OF STRAPPING OPTION		STRAP REQUIRED	STRAP POSITION
Character printed when received with parity error.	Diamond ◇ printed (CINT J18 must be out)	J10, J18, J15	IN
		J11, J19, J14	OUT
	Nothing printed - not even a space.	*J10, J19	IN
		*J11, J18	OUT
		J11, J19	IN
		J10, J18	OUT
	Character printed as received	J11, J18	IN
		J10, J19	OUT
Received Delete Code	Resets Printer Logic (CINT J18 Must be in)	J14	IN
		J15	OUT
	Code is ignored.	*J14	OUT
		*J15	IN
Baud Rate Clock Selection	External Clock	J29	IN
		J20, J21, J22, J23, J26, J27, & J28	OUT
	150 Baud	J28	IN
		J20, J21, J22, J23, J26, J27, & J29	OUT
	300 Baud	J27	IN
		J20, J21, J22, J23, J26, J28, & J29	OUT
	600 Baud	J26	IN
		J20, J21, J22, J23, J27, J28, & J29	OUT
	1200 Baud	J20	IN
		J21, J22, J23, J26, J27, J28, & J29	OUT
	2400 Baud	J21	IN
		J20, J22, J23, J26, J27, J28, & J29	OUT
Baud Rate Clock Selection.	4800 Baud	J22	IN
		J20, J21, J23, J26, J27, J28, & J29	OUT
	9600 Baud	*J23	IN
		*J20, J21, J22, J26, J27, J28, * J29	OUT

*Standard strapping configuration shipped from the factory.

(TABLE 5-5 CONTINUED)

DESCRIPTION OF STRAPPING OPTION		STRAP REQUIRED	STRAP POSITION
Parity Detection	Even	J30	IN
		J31, J32	OUT
	Odd	J31	IN
		J30, J32	OUT
	No Check	*J32	IN
		*J30, J31	OUT
BUSY signal status when Printer cannot receive data.	EIA Negative. TTL Low. No current in Loop.	*J24	IN
		*J25	OUT
	EIA positive. TTL High. Current in Loop.	J24	OUT
		J25	IN
Allows EIA or Current Loop configuration with TTL level external Baud Rate Clock, and with data sampling at high to low transition.		*J33	IN
		*J34	OUT
Same as above except data sampling is at low to high transition.		J33	OUT
		J34	IN
Allows EIA or Current Loop configuration with TTL received data signal at low level for binary 1(start bit high)		*J35	OUT
		*J36	IN
Same as above except TTL received data signal at high level for binary 1 (start bit low)		J35	IN
		J36	OUT
BUSY signal transition	Middle of stop bit	J37	IN
		J38	OUT
	Middle of parity bit	*J37	OUT
		*J38	IN
Parity Error signal duration.	Middle of stop bit of erroneous character to middle of start bit of next character.	*J39	IN
		*J40	OUT
	Middle of parity bit to middle of stop bit of erroneous character.	J39	OUT
		J40	IN

*Standard strapping configuration as shipped from the factory.

(TABLE 5-5 CONTINUED)

CINT STRAPPING
The strapping of the Unbuffered Parallel Interface (CINT) cirucit board is described in GEK49271. When the CINT is used in conjunction with the SAUX, its strapping is arranged as explained below: To allow Unbuffered Closed Loop Serial Operation: Straps J1, J3, J10, J16, J19, J28, J6, & J36 must be IN Straps J2, J4, J17, J20, J27, J7, & J35 must be OUT In addition to the above requirements, normal strapping (as shipped from the factory) of the remaining straps are: J12, J14, J21, J29, & J31 IN* J13, J15, J18, J22, J30 & J32 OUT*

*Standard strapping configuration as shipped from the factory.

TEST POINT DATA

The SAUX contains two test points along the front edge of the circuit board. The table below (Table 5-6) details the information which is available at these test points.

TABLE 5-6

TEST POINT INFORMATION

TEST POINT	INFORMATION AVAILABLE
1	Monitors the first stage of the Series to Parallel Converter circuit.
2	Monitor the baud rate clock used to clock the serial data into the SAUX circuit board.

TROUBLE SYMPTOMS

In addition to the trouble symptoms which are given in GEK-35997, GEK-49271, and the appropriate Printer srevice manual, a defective SAUX could cause problems with symptoms such as those listed in Table 5-4.

TABLE 5-7

DEFFECTIVE SAUX SYMPTOMS

1. Printer sends constant BUSY signal to data source, or Printer never sends BUSY signal to data source.
2. Constant FAULT and LOW PAPER condition.
3. Garbled data flow. No data flow.
4. Printer will not clock serial data through Interface. Printer will not accept external buad rate clock from the data source.
5. Printer will not detect parity errors when strapped to do so.

SERVICE DRAWINGS

Service Drawings which pertain to the HINT or CINT Interface boards are contained in GEK-35997 or GEK-49271. Service Drawings for the Printer are contained in its service drawing package. Special drawings which pertain to the SAUX are contained herein. They are as follows:

Connection Diagram
for Mother Board . . . . . 44D400355, Sh. 3

Wiring Diagram for SAUX. 44D401707

ACCO USA
WHEELING, ILLINOIS 60090
25077
0 50505 25077 6
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TANGERINE/TANGERINE/ANARANJADO

MP MASTER
MA32653